REMARKS

The following remarks are responsive to the Office Action mailed July 2, 2007.

Claims 1-17 are pending in the present application.

The Examiner has considered Applicant's amendment dated January 2, 2008; but is considered moot in view of the new grounds of rejection.

Claim Rejection under 35 USC 102:

The Examiner rejects Claims 1, 2, 4-6, and 9-11 under 35 USC section 102(e) as being anticipated by Rho (USPAP 2004/0169807).

Claim 1:

Specifically, as to Claim 1, the Examiner finds that Rho discloses a method of subpixel rendering input image data onto a display panel, said input image data comprises image data formatted for a first subpixel layout and wherein said display panel comprises a second subpixel layout further comprising a repeating grouping of a plurality of primary colored subpixels and said second subpixel layout is different from said first subpixel layout (see Fig. 4A, 5A of Rho), the steps of said method comprising:

subpixel rendering input image data that is input at a first clock rate (see paragraph 0178, CPV);

outputting subpixel rendered data to said display panel at a second clock rate (see paragraph 0178, HCLK).

As Claim 1, Applicant respectfully traverses the present rejection.

Applicant reproduces Figs. 4A and 5A – as well as paragraphs [0176]-[0183] – of Rho below for the convenience of the Examiner:

R	B	G	R	B	G
G	B	R	G	B	R
R	B	G	R	B	G
G	B	R	G	B	R

Figure 4A

B	R	G	B	R	G
G	R	B	G	R	B
B	R	G	B	R	G
G	R	B	G	R	B

Figure 5A

"[0176] Now, the operation of the LCD will be described in detail.

[0177] The signal controller 600 is supplied with RGB image signals R, G and B and input control signals controlling the display thereof such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a main clock MCLK, and a data enable signal DE, from an external graphic controller (not shown). After generating gate control signals CONT1 and data control signals CONT2 and processing the image signals R, G and B suitable for the operation of the panel assembly 300 on the basis of the input control signals and the input image signals R, G and B, the signal controller 600 provides the gate control signals CONT1 for the gate driver 400, and the processed image signals R', G' and B' and the data control signals CONT2 for the data driver 500.

[0178] The gate control signals CONT1 include a vertical synchronization start signal STV for informing of start of a frame, a **gate clock signal CPV for controlling the output time of the gate-on voltage Von,** and an output enable signal OE for defining the width of the gate-on voltage Von. **The data control signals CONT2 include a horizontal synchronization start signal STH for informing of start of a horizontal period, a load signal LOAD or TP for instructing to apply the appropriate data voltages to the data lines D1-Dm, an inversion control signal RVS for reversing the polarity of the data voltages (with respect to the common voltage Vcom) and a data clock signal HCLK.**

[0179] The data driver 500 receives a packet of the image data R', G' and B' for a pixel row from the signal controller 600 and converts the image data R', G' and B' into the analogue data voltages selected from the gray voltages supplied from the gray voltage generator 800 in response to the data control signals CONT2 from the signal controller 600.

[0180] Responsive to the gate control signals CONT1 from the signals controller 600, the gate driver 400 applies the gate-on voltage Von to the gate line G1-Gn, thereby turning on the switching elements Q connected thereto.

[0181] The data driver 500 applies the data voltages to the corresponding data lines D1-Dm for a turn-on time of the switching elements Q (which is called "one horizontal period" or "1H" and equals to one periods of the horizontal synchronization signal Hsync, the data enable signal DE, and the gate clock signal CPV). Then, the data voltages in turn are supplied to the corresponding pixels via the turned-on switching elements Q.

> [0182] The difference between the data voltage and the common voltage Vcom applied to a pixel is expressed as a charged voltage of the LC capacitor CLC, i.e., a pixel voltage. The liquid crystal molecules have orientations depending on the magnitude of the pixel voltage and the orientations determine the polarization of light passing through the LC capacitor CLC. The polarizers convert the light polarization into the light transmittance.
>
> [0183] By repeating this procedure, all gate lines G1-Gn are sequentially supplied with the gate-on voltage Von during a frame, thereby applying the data voltages to all pixels. When the next frame starts after finishing one frame, the inversion control signal RVS applied to the data driver 500is controlled such that the polarity of the data voltages is reversed (which is called "frame inversion"). The inversion control signal RVS may be also controlled such that the polarity of the data voltages flowing in a data line in one frame are reversed (which is called "line inversion"), or the polarity of the data voltages in one packet are reversed (which is called "dot inversion")." (Rho, **bold** emphasis added).

Applicant reproduces the above paragraphs of Rho above and points out to the Examiner that the entire discussion concerns how **output image data** is finally clocked to the panel for rendering – and does not disclose the present invention of Claim 1.

As an initial observation, Rho (which is assigned to Samsung) is concerned with panels having different subpixel layouts. This is seen most clearly in paragraph 0007 – which discusses Clairvoyante Laboratories "PenTile Matrix" layouts. "PenTile Matrix" is a trademark of the assignee of the present application. Therefore, Rho does disclose panels of the type disclosed in the present application. Since the previous Office Action in this present application, Samsung has now acquired substantially all of the assets of Clairvoyante, Inc. – including the present application.

Secondly, however, Rho does not disclose how to input image data of a first subpixel layout (e.g. image data that is meant to be rendered on a conventional RGB striped panel) and subsequently "subpixel render" that input image data – so that the proper image data may be sent to the display (that is, a display having a different, "second subpixel layout") in a manner that keeps the image intact for the viewer.

To see that this is so, Applicant reproduces for the convenience of the Examiner paragraphs [0078] to [0084] of Park that contains the only discussion that Applicant finds relevant to the issue of mapping input image data of a first subpixel format into output image data of a second subpixel format.

[0078] An LCD having the above-described pixel arrangement are rendered for increasing resolution and this will be described in detail with reference to FIG. 6.

[0079] FIG. 6 is an exemplary pixel group for a rendered LCD according to an embodiment of the present invention.

[0080] Referring to FIG. 6, an exemplary pixel group for rendering is centered on any pixel P1 in a bicolor pixel. The pixel group includes four pixels P2 in bicolor columns and two pixels in a unicolor column, which are adjacent to the center pixel P1. The rendering may give about half weight to the center pixel P1.

[0081] In the meantime, since the pixels representing the same colors in bicolor columns face each other obliquely in a symmetrical manner as shown in FIGS. 4B, 5B and 6 and are seen as mixed. On the contrary, the pixels in unicolor columns are arranged in stripes and do not make symmetry with the pixels in the bicolor columns, which may cause incomplete color mixture and deteriorate image quality. In particular, the bicolor columns shown in FIG. 4B represent green and red, which are mixed to form yellow. Since yellow has luminosity higher than blue, the bicolor columns may be seen brighter than the unicolor columns. On the contrary, blue and green in the bicolor columns shown in FIG. 5B are mixed to form cyan, which has similar luminosity to red, and thus the brightness difference may not be detected.

[0082] The brightness difference may be much reduced by differentiating saturation of two pixels in two adjacent red pixels R in a unicolor column shown in FIG. 5B.

[0083] For example, the saturation of a red pixel R right to a blue pixel B and left to a green pixel G is lower than that of a red pixel R left to a blue pixel B and right to a green pixel G. The red pixel R right to a relatively dark, blue pixel B has lower saturation but higher luminosity than the blue pixel B, while the red pixel B right to a relatively bright, green pixel G has higher saturation but lower luminosity than the green pixel G. Accordingly, the brightness difference between two adjacent pixels in the row direction and the column direction is reduced.

[0084] The saturation difference may be obtained by differentiating the amount of pigment mixed to photoresist to form color filters 230 shown in FIG. 1. However, other methods may be also used for the saturation difference.

As may be seen by the above excerpt, Rho does not consider the issue of the timing of such a mapping from a first format to a second format. In fact, Applicant finds this excerpt – which contains the only discussion about mapping input into output data – as supporting the argument that paragraph [0178] of Rho above is merely discussing timing signals to send output data (already formatted) out to the display.

Not only does Rho not disclose this, Rho does not go further with the claim limitations of Claim 1 wherein said **input** image data is input at a **first clock rate** and the **output** image data is output to the display at a **second clock rate**.

The Examiner cites Rho at paragraph 0178 (as reproduced above) and Applicant notes that Rho is actually describing only how **output** image data is sent to the display – which requires two clocked signals – a gate signal and a data signal. This is true of nearly every LCD display – whether it comprises a novel subpixel layout or is a conventional RGB stripe layout.

However, as Rho is not disclosing many of the salient limitations of Claim 1, Applicant respectfully traverses the present rejection to Claim 1 and respectfully asks that the Examiner reconsider the present rejection.

Claims 2-6 and 9-11:

As Claims 2-6 and 9-11 ultimately depend from allowable Claim 1, Applicant respectfully avers that these Claims are themselves allowable – without recourse to any additional and separate argument for their patentability.

Claim Rejections Under 35 USC 103:

The Examiner rejects Claims 3, 7, 8 and 14 under 35 USC section 103(a) as being unpatentable over Rho in view of Park (USP 6,160,535).

The Examiner states – in all Claims rejected herein – that Rho discloses the method of Claim 1 above.

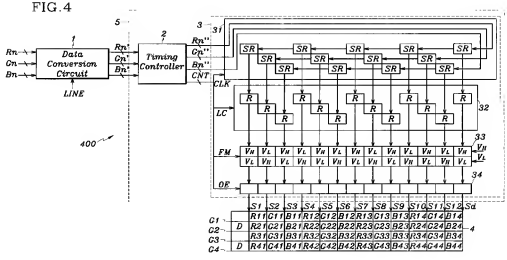
As Applicant respectfully traverses the Examiner's use of Rho vis-à-vis Claim 1 above, Applicant respectfully traverses the present rejection to Claims 3, 7, 8 and 14 – as the same rationale for Claim 1 applies with equal force for these Claims.

Claim 3:

In addition, with respect to Claim 3, Applicant respectfully disagrees with the application of Park, as applied in combination with Rho.

For the convenience of the Examiner, Applicant reproduces the Figure 4 of Park below:

FIG. 4



As may be seen from Figure 4, Park has the designation "D" – seemingly in the data stream that is output to the display.

However, Park uses dummy data – inserted only at the edge of the panel display for a "dummy line" – only to perfect a polarity inversion scheme on the display, and not to match an image conversion from an input image data stream (for a display designed for a first subpixel

layout) to an output image data stream for a display designed for a second subpixel layout. In fact, it appears to Applicant that Park is employing this dummy data for the purposes of effecting a proper polarity inversion on the output panel. This is seen in the following excerpt of Park:

> Applying voltages having the same polarity to a liquid crystal cell can cause an electrochemical change in the pixel electrode and the common electrode due to precipitation of ionic impurities from the liquid crystal material. This change can significantly reduce display sensitivity and brightness. Accordingly, it is generally desirable to periodically invert the polarity of the voltage applied to the liquid crystal cell in order to prevent this phenomenon.
>
> As illustrated in FIGS. 1B-1C, a conventional dot inversion driving technique involves applying data line voltages that have different polarities to adjacent pixel electrodes, for example, by driving alternating pixel elements with negative (hatched) and positive (no hatching) voltages. Typically, the polarity of the voltages applied to a given pixel electrode is inverted at each frame, as illustrated by FIGS. 1B and FIG. 1C, which illustrate inversion between a first frame (FIG. 1B) and a second frame (FIG. 1C). FIG. 2 illustrates how a data line voltage applied during a frame F inverts with each line period H with respect to a 5V signal used to drive the common electrode of the cell. The data line is driven by voltages from 0V to 10V to provide the appropriate polarity for the pixel electrodes connected thereto. The specified voltage values are used only as examples -0V, 5V and 10V. In actuality, the voltage values depend on panel characteristics.
>
> Although the above-mentioned conventional dot-inversion driving technique may improve display characteristics, such a technique may be disadvantageous because the polarity of the data line voltage is inverted after each horizontal line period. Switching operations typically are required to achieve the inversion, which can lead to undesirably high power consumption. Furthermore, each voltage inversion may require a significant amount of time and may lead to insufficient charging of the cell after each inversion, resulting in poor display performance. (Park at col. 1, line 52 to col. 2, line 19).

For the convenience of the Examiner, Applicant reproduces below the following excerpt of Park in his discussion about Figure 4 -- as well as the excerpt cited by the Examiner at col. 6, line 61 to col. 7, line 9:

> FIG. 4 illustrates a controller 400 for driving a liquid crystal panel 4 of the type illustrated in FIGS. 3A-3C. The controller 400 includes a data conversion circuit

1, as well as a driving circuit 5 that includes a timing controller 2 and a source driving circuit 3. As illustrated, the color liquid crystal panel 4 has a resolution of 4.times.4, and is controlled by four gate lines G1-G4 and thirteen data lines S1-S12, Sd. Each pixel electrode is labeled with a designation R11, R21, . . . , B34, B44 of the color component to be displayed thereby.

The data conversion circuit 1 reformats color signals Rn, Gn and Bn, which preferably are standard format color video signals generated by a graphics controller such as one of the type commonly employed in personal computers. The data conversion circuit 1 produces reformatted color signals Rn', Gn', Bn' that are compatible with the structure of the panel 4, responsive to a line period signal LINE. As illustrated in FIG. 6, the color signals Rn, Gn and Bn each have a serial data format including a line period L including sequences of color values separated by line blanking intervals LB. For example, the red color signal Rn includes color values R11, R12, R13, R14, . . . R41, R42, R43, R44, the green color signal Gn includes color values G11, G12, G13, G14, . . . G41, G42, G43, G44, and the blue color signal Bn includes the color values B11, B12, B13, B14, . . . B41, B42, B43, B44. A frame period F is demarcated by a frame blanking period FB, and includes a plurality of line periods L demarcated by line blanking periods LB, corresponding to transition of the line period signal LINE. The reformatted signals Rn', Gn', Bn' have a similar line and frame period structure, but the arrangement of color values therein are modified such that each of reformatted color signals Rn', Gn', Bn' represents a multiplexing of color values for adjacent columns in the panel 4. **In addition, dummy values D are inserted into the color value sequences for the first reformatted color signal Rn', for driving the dummy line Sd.** (Park at col. 5, line 38 to col. 6, line 6) (**Bold** emphasis added).

The shift register 31 has three data transmission paths, each transmission path including a plurality of shift registers SR which are serially connected. The data transmission path for the first buffered reformatted color signal Rn" includes five shift registers. The data transmission paths for the second and third buffered reformatted color signals Gn", Bn" signal line each include four shift registers. **The path for the Rn' signal line utilizes an additional shift register due to the presence of the dummy data line Sd.** Each data transmission path assigns the color values in the sequence of color values in the buffered reformatted color signals Rn", Gn" , Bn" by shifting the data of each color signal sequentially in response to the clock signal CLK. The output from each shift register is provided to the latch 32. The latch 32, which includes a plurality of registers R, is responsive to the latch control signal LC, latching data at each line period. (Park at col. 6, line 61 to col. 7, line 9) (**bold** emphasis added).

As Park is not employing dummy data to convert the input image data stream (of a first subpixel layout) to an output data stream (of a second subpixel layout), Park adds nothing to the combination that dummy data has been used for other reasons not related to the present application.

As the collection of Rho and Park, either singly or in combination, does not meet the limitations of Claim 1 (as discussed above) or Claims 3, Applicant respectfully avers that Claim 3 is patentable over the combination of Rho and Park.

Claims 7 and 8:

With respect to Claims 7 and 8, Applicant avers that the argument made above, for the application of Rho to Claim 1 and the combination of Rho and Park as applied to Claim 3, applies with equal force to Claims 7 and 8.

In particular, the buffering referred to by the Examiner at element 34 in Figure 4 of Park adds nothing more than adding dummy data for unrelated reasons (i.e. polarity inversion) has been used.

Applicant respectfully avers that Claims 7 and 8 are patentable over the combination of Rho and Park, either singly or in combination.

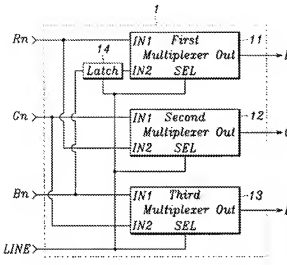
Claim 14:

As to Claim 14, the Examiner applies Rho (as applied to Claim 1); however, the Examiner finds that Rho does not teach a channel formatter for effectively ordering said output data; and a means for outputting the data formatted by said channel formatter to said display.

However, the Examiner finds that Park discloses an LCD wherein Park teaches the use of a channel formatter.

For the convenience of the Examiner, Applicant reproduces Figure 5 of Park below:

FIG.5



Applicant draws the Examiner's attention to the except of Park at col. 6, line 61 to col. 7, line 9 above – as cited by the Examiner in support of his rejection of Claim 14.

As to currently amended Claim 14, Applicant respectfully traverses the present rejection.

Claim 14, as now amended, has the limitation that the system comprises a channel formatter … that [affects] a timing scheme to map input image data of one subpixel layout format to output data of a second subpixel layout format.

As Applicant has argued above that Rho does not disclose such a timing scheme – and that Park does not supply the deficit, Applicant respectfully submits that Claim 14, as amended, is patentable over Rho and Park of record – either singly or in combination.

Claims 15, 16 and 17:

As Claims 15, 16 and 17 ultimately depend from allowable Claim 14, Applicant avers that Claims 15, 16 and 17 are themselves allowable – without recourse to separate argument for their patentability. Applicant reserves all such argument for future responses if needed.

Claims 12-13:

The Examiner rejects Claims 12 and 13 under 35 USC 103(a) as being unpatentable over Rho and Park in further view of Furuhashi (USP 6,340,970).

The Examiner finds that Rho and Park disclose a method of subpixel rendering input image data onto a display panel, said input image data comprises image data formatted for a first subpixel layout and wherein said display panel comprises a second subpixel layout further comprising a repeating grouping of a plurality of primary colored subpixels and said second subpixel layout is different from said first subpixel layout, the steps of said method comprising:

outputting subpixel rendered data to said display panel in a format wherein dummy data is inserted into the output data.

As to Claim 12, as currently amended, Applicant respectfully traverses the present rejection.

Applicant avers that the argument above that Rho and Park do not teach (either singly or in combination) the application of dummy data to affect a timing scheme to map said input image data formatted for said first colored subpixel layout onto said output data formatted for said second colored subpixel applies with equal force to the present rejection to Claim 12 as currently amended.

Applicant respectfully requests the Examiner to reconsider the present rejection and pass Claims 12 and 13 to allowance.

Conclusion

Based on the foregoing reasons, all Claims, pending after this amendment, are now in condition for allowance. Please telephone the undersigned attorney at (408) 392-9250 if there are any questions.

Respectfully submitted,

Dated: July 15, 2008

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I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office (USPTO) via the USPTO's EFS-Web electronic filing system on July 15, 2008.

/Carolyn Marsden/ July 15, 2008
Carolyn Marsden Date of Signature